

# 大同大學 九十二 學年度 轉學考試 試題

考試科目：電子學

系別：電機工程學系

共 1/1 頁

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

BJT:  $|V_{BE}|(\text{active})=0.7\text{V}$ ,  $|V_{BE}|(\text{sat})=0.8\text{V}$ ,  $|V_{CE}|(\text{sat})=0.2\text{V}$ ; MOSFET:  $|V_t|$  threshold voltage.

1. For the circuit in Fig. p1,  $R_1=10\text{K}\Omega$ ,  $R_2=1\text{K}\Omega$ , calculate  $V_B$  and  $V_E$  for  $V_I=3\text{V}$ , and  $-5\text{V}$ . Both BJTs have  $\beta=100$ .(20%)

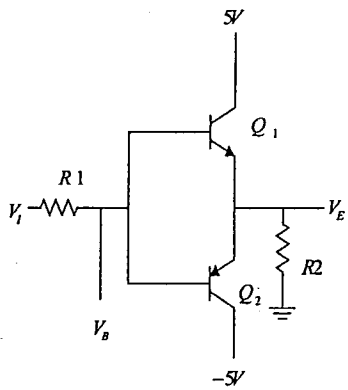


Fig. p1

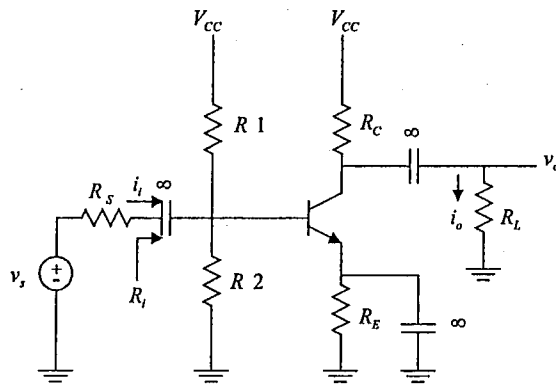


Fig. p2,

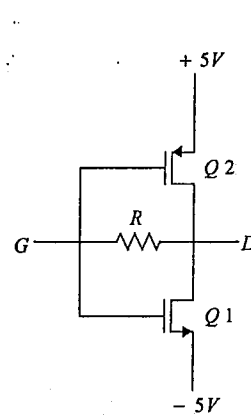


Fig. p3

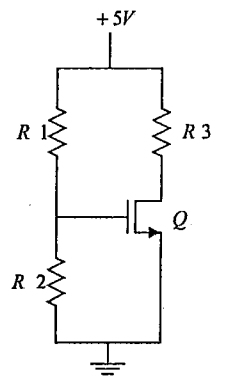


Fig. p4

2. For the circuit shown in Fig. p2, let  $V_{CC}=9\text{V}$ ,  $R_1=27\text{K}\Omega$ ,  $R_2=15\text{K}\Omega$ ,  $R_E=1.2\text{K}\Omega$ ,  $R_C=2.2\text{K}\Omega$ . The BJT has  $\beta=100$  and Early voltage  $V_A=100\text{V}$ . (in part(a), neglect Early effect)
- (a). Calculate the dc bias current  $I_E$ . (10%)
- (b). If the amplifier operates between a source for which  $R_s=10\text{K}\Omega$  and load  $R_L=2\text{K}\Omega$ , calculate the input resistance  $R_i$ , the voltage gain  $v_o/v_s$ , and the current gain  $i_o/i_i$ . (15%)
3. The MOSFETs in the circuit of Fig. p3 are matched, with  $\mu_n C_{ox} (\frac{W}{L})_1 = \mu_p C_{ox} (\frac{W}{L})_2 = 50 \mu\text{A}/\text{V}^2$  and  $|V_t|=2\text{V}$ , the resistance  $R=10\text{M}\Omega$
- (a). For G and D open, calculate the drain current  $I_{D1}$  and  $I_{D2}$ ? (8%)
- (b). Through a large coupling capacitor, G is driven from a source  $v_i$  having a resistance of  $1\text{M}\Omega$ , calculate the voltage gain  $v_d/v_i$ , assuming both MOSFETs with  $\frac{1}{|\lambda|} = |V_A| = 180\text{V}$ . (12%)
4. For the circuit in Fig. p4, nMOS with  $V_t=1\text{V}$  and  $\mu_n C_{ox} \frac{W}{L} = 0.2 \text{mA}/\text{V}^2$ ;  $R_1=30\text{K}\Omega$ ,  $R_2=20\text{K}\Omega$ ,  $R_3=20\text{K}\Omega$ , determine the transition point parameters  $V_{GS,t}$  and  $I_{D,t}$ . (Here, transition point means:  $V_{GS} < V_{GS,t}$ ,  $Q$  in the saturation region;  $V_{GS} > V_{GS,t}$ ,  $Q$  in linear region.) (13%)
5. (a). Draw the CMOS inverter circuit and indicate the pMOS and nMOS. (4%)
- (b). Sketch the CMOS inverter VTC, i.e.  $V_o$  vs  $V_i$  plot and indicate  $V_{IL}$ ,  $V_{IH}$ ,  $V_{OH}$ ,  $V_{OL}$ . Define the noise margin  $NM_H$  and  $NM_L$ . (12%)
- (c) Draw the two inputs CMOS NAND and NOR circuits and indicate pMOS and nMOS clearly. (8%)