大同大學 102 學年度 轉學入學考試試題

考試科目:電子學　　所別:電機工程學系　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. In Fig.1, diode cut-in voltage $V_{D0}=0.6V$, diode resistance $r_D=0\Omega$, for the following cases, calculate the output voltage V_O. (a) $V_1=V_2=5V$ (b) $V_1=5V, V_2=0V$ (c) $V_1=V_2=0V$ (18%)

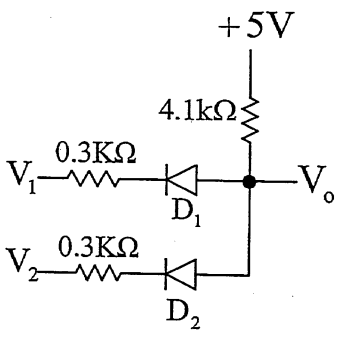

Fig. 1

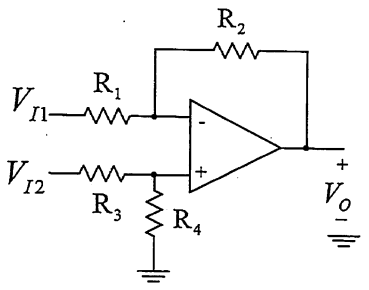

Fig. 2

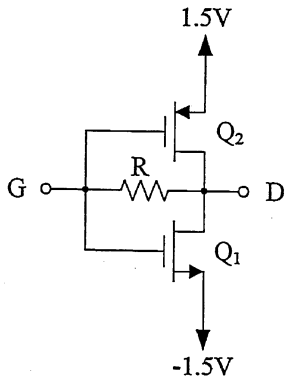

Fig. 3

2. (a). For the ideal OP in Fig. 2, derive the output V_O in terms of V_{I1}, V_{I2} and resistors. (12%)
   (b). To relize the circuit as a difference amplifier, i.e. $V_O=A(V_{I2}-V_{I1})$, derive the relationship among the resistors R_1, R_2, R_3,and R_4, define the gain factor A. (8%)

3. The MOSFETs in the circuit of Fig. 3 are matched, having $\mu_n C_{ox}(W/L)_n=\mu_p C_{ox}(W/L)_p=1mA/V^2$, $V_{tn}=|V_{tp}|=0.5V$, and the resistance R=1MΩ
   (a). For G and D open, calculate the dc voltage at G (V_G) and dc drain current I_{D1} (Q_1) and I_{D2} (Q_2). (8%)
   (b). For finite r_o ($\frac{1}{|\lambda|}=|V_A|=20V$, for both n and p MOS), draw the small-signal equivalent circuit, calculate the voltage gain (v_d/v_g) from G to D and find the input resistance (R_{in}) at G.(12%)

4. Refer to Fig. 4, BJT β=100, for the differential mode, $v_1=0.5v_{id}, v_2=-0.5v_{id}$, draw the half circuit (3%), calculate the voltage gain $A_d=\frac{v_{c2}-v_{c1}}{v_{id}}$ (12%) and input resistance R_{id}.(5%)

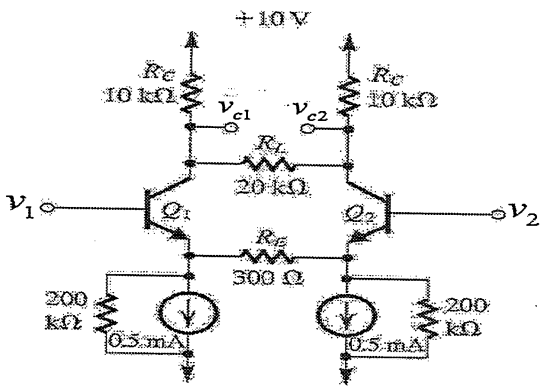

Fig. 4

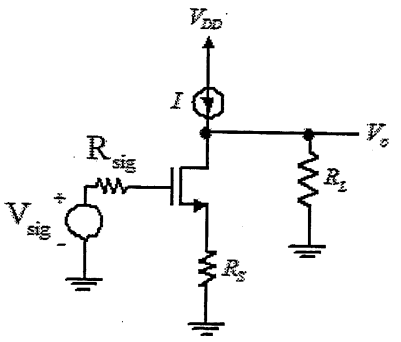

Fig. 5

5. (a). For the circuit in Fig. 5, the coupling capacitances are not shown, the current source is ideal, MOS $r_o=\infty$, derive the midband voltage gain $A_M=V_o/V_{sig}$.(10%)
   (b). Draw the small-signal circuit including C_{gs} and C_{gd}, use OCTC (open circuit time constant) method to derive the time constants τ_{gs}, τ_{gd}, for C_{gs}, C_{gd}. (8%%)
   (c). Follows part (a),(b) write an expression for the transfer function of the voltage gain $A(s)=V_o/V_{sig}$, define the pole frequency (ω_p) in terms of τ_{gs} and τ_{gd}.. (4%)